Notice of Allowability	Application No.	Applicant(s)	
	10/707,870	WANG, TAI-HO	
	Examiner	Art Unit	
	Scott Bauer	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment of 1/26/2006*.

2. ☒ The allowed claim(s) is/are *1-12*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see pages 7-13 of the amendment, filed 01/26/2006, with respect to Claims 1-11 have been fully considered and are persuasive. The rejection of Claims 1-11 has been withdrawn.

Reasons for Allowance

1. Claims 1-12 are allowed.

2. The following is an examiner's statement of reasons for allowance:

3. Claim 1 is allowable because the prior art of record does not teach or fairly suggest an ESD protection circuit comprising: a first common conductive line; a first diode, a cathode of the first diode coupled to the first common conductive line, an anode of the first diode coupled to the first system voltage; a first P-type transistor, a first S/D terminal and a gate terminal of the first P-type transistor coupled to the first system voltage, a second S/D terminal of the first P-type transistor coupled to the first pad; and a first N-type transistor, a first S/D terminal of the first N-type transistor *directly* coupled to the first common conductive line, a gate terminal of the first N-type transistor coupled

to the first ground voltage, a second S/D terminal of the first N-type transistor coupled to the first pad.

Applicant has amended the claim to include the limitation that the first S/D terminal of the first N-type transistor is directly coupled to the first common conductive line. As applicant states in arguments, the first S/D terminal of the first n-type transistor is coupled to a resistor and is not directly coupled to a system voltage. As the resistor is needed to provide the coupling function as described by Applicant, it would not have been obvious to remove the resistor in view of the prior art of record and would teach away from Chen et al. As such Chen et al. does not teach the ESD protection circuit of amended Claim 1.

4. Claims 2-6 are allowable as they depend from Claim 1, which is also allowable.

5. Claim 7 is allowable because the prior art of record does not teach or fairly suggest an electrostatic discharge (ESD) protection circuit coupled to a first pad of an integrated circuit having a plurality of system voltage sets, the system voltages including a first ground voltage, the ESD protection circuit comprising: a first common conductive line; a first diode, a cathode of the first diode coupled to the first ground voltage, an anode of the first diode coupled to the first common conductive line; and a first N-type transistor, a first S/D terminal of the first N-type transistor coupled to the first pad, a gate terminal and a substrate terminal of the first N-type transistor coupled to the first ground voltage, a second S/D terminal of the first N-type transistor coupled to the first

common conductive line. As stated in Applicants arguments, the rejection made of Claims 7 & 8 fail to establish prima facie case of obviousness to teach Applicant's invention. Further no prior art of record teaches the ESD protection circuit of Claim 7.

Gauthier Jr. et al. (US.6,256,184) teaches an ESD protection circuit wherein a FET is coupled between an I/O pad and ground. However, Gauthier Jr. et al. teaches that the diode is connected is reverse bias to the diode of Claim 7 and that the gate terminal of the FET is connected to the common conductive line instead of the ground voltage and that the S/D terminal is connected to the ground voltage instead of the common conductive line. As such, there is no motivation to combine the reference with Chen et al.

6. Claims 8-10 are allowable as they depend from Claim 7, which is also allowable.

7. Claim 11 is allowable because the prior art of record does not teach or fairly suggest a first N-type transistor, a first S/D terminal of the first N-type transistor directly coupled to the system voltage, a gate terminal of the first N-type transistor coupled to the ground voltage. a second S/D terminal of the first N-type transistor coupled to the pad. As discussed above in Claim 1. Applicant has amended the claim to overcome the rejection of the previous office action. Chen et al does not teach that a first S/D terminal of the first N-type transistor is directly coupled to the system voltage.

8. Claim 12 is allowable as it depends from Claim 11, which is also allowable.

9. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Bauer whose telephone number is 571-272-5986. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAB
4/3/2006

PHUONG T. VU
PRIMARY EXAMINER